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Page 1 of 10

DATE: 12-11-03

FROM: <i>Cindy Dees</i> COMPANY NAME: TEXAS INSTRUMENTS INCORPORATED PHONE NUMBER: (972) 917- FAX NUMBER: (972) 917-4418	TO: <i>Mary Wilczewski</i> COMPANY NAME: <i>USPTO</i> PHONE NUMBER: FAX NUMBER: <i>703-746-4071</i>
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MESSAGE

The attached is being sent pursuant to your request to Jim Brady with Texas Instruments.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/988,686	12/11/1997	ANTHONY J. KONECNI	TI-22166	7837

23494 7590 11/19/2002

TEXAS INSTRUMENTS INCORPORATED
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EXAMINER

WILCZEWSKI, MARY A

ART UNIT

PAPER NUMBER

2822

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Please find below and/or attached an Office communication concerning this application or proceeding.

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PTO-90C (Rev. 07-01)

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ART UNIT

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28

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Commissioner of Patents and Trademarks

The reply brief filed September 4, 2002, has been entered and considered. The application has been forwarded to the Board of Patent Appeals and Interferences for decision on the appeal.

An English-language translation of Masanori JP4-171744 is attached.

Any inquiry concerning this communication should be directed to M. Wilczewski at telephone number 703-308-2771.

M. Wilczewski
Primary Examiner
Tech Center 2800

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PTO 02-3523

Japanese Kokai Patent Application No.
Hei 4[1992]-171744

METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE

Naohiko Takeshita, et al.

UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. JULY 2002
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METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

[Handotai sochi no seizo hoho]

Inventors: Naohiko Takeshita, et al.

Applicant: Mitsubishi Electric Corp.

Agent: Masuo Oiwa, patent attorney, and
2 others

[There is no amendment to this patent.]

Claim

A method for manufacturing a semiconductor device which involves a step in which a base layer provided with a lower aluminum wiring layer is prepared, a step in which an interlayer insulating film having contact holes at prescribed positions is formed on the aforementioned base layer,

a step in which dry etching cleaning is applied to the aforementioned lower aluminum wiring layer exposed via the aforementioned contact holes using a mixed gas including a rare gas and a hydrogen gas, and

a step in which an upper wiring layer is formed on the aforementioned interlayer insulating film while achieving electrical connection with the aforementioned lower aluminum wiring layer via the aforementioned contact holes.

Detailed explanation of the invention

Industrial application field

The present invention pertains to a method for manufacturing a semiconductor device in which a lower aluminum wiring layer and an upper wiring layer are connected via contact holes.

Prior art

Usually, a semiconductor device has an aluminum multi-layer wiring structure. Figure 2 is a cross section of a conventional semiconductor device having such an aluminum multi-layer wiring structure.

Next, the method for manufacturing the semiconductor device shown in Figure 2 will be described. First, first interlayer insulating film 2 is formed on silicon substrate 1, and contact holes are created. Then, lower aluminum wiring layer 3 is formed in a pattern to achieve electrical connection with silicon substrate 1 via said contact holes. Next, second interlayer insulating film 4 is formed on lower wiring layer 3. Then, a photoresist is formed by means of a phototype processing method over the entire area except the parts where the contact holes are created, and second insulating film 4 is removed selectively by means of a taper etching method, a combination of wet etching utilizing fluoric acid and reactive ion etching utilizing CHF_3 and O_2 as primary ingredient gases, using said photoresist as a mask in order to create electrical connection parts (will be referred to as via-hole parts, hereinafter), that is, contact holes for achieving electrical connection between lower aluminum wiring layer 3 and upper aluminum wiring layer 5 to be formed later.

Reaction products created during the photoresist formation and the etching are removed after the etching is completed using an oxygen plasma or a wet chemical processing method. Because lower aluminum wiring layer 3 is exposed to plasma from a fluorine type gas, such as CHF_3 , or gaseous oxygen through the via-holes during the via-hole creating process, degenerated aluminum layer (fluoride or oxide) 6 is formed to a thickness of 100 Å or so on the surface of lower aluminum wiring layer 3.

Next, said degenerated layer 6 is removed by means of sputtering etching utilizing an argon gas plasma. This is done in order to keep the contact characteristic between lower aluminum wiring layer 3 and upper aluminum wiring layer 5 good.

Next, upper aluminum wiring layer 5 is formed in a vacuum by means of the sputtering method while achieving electrical connection with lower aluminum wiring layer 3 via the via-hole parts, and a pattern is created by means of the phototype processing method and an etching method. A film made of an aluminum alloy, such as Al-Si, Al-Si-Cu, or Al-Cu, is utilized for upper aluminum wiring layer 3 [sic; 5].

Furthermore, a heat treatment at around 400-450°C is applied in order to improve the mixing condition of lower aluminum wiring layer 3 with upper aluminum wiring layer 5 at the via-hole areas.

Problem to be solved by the invention

The conventional semiconductor device was created according to the aforementioned process; wherein, the removal of degenerated layer 6 is achieved using a physical method called sputtering etching utilizing an argon gas plasma. Thus, removed particles of degenerated layer 6 adhered back to the surface of lower aluminum wiring layer 3, creating a problem that the contact resistance with lower aluminum wiring layer 3 increased, and the reliabilities of the electromigration tolerance and the stress migration tolerance at the via-holes deteriorated when upper aluminum wiring layer 5 was formed.

The present invention was made to solve the aforementioned problem, and its purpose is to realize a method for manufacturing a semiconductor device with little contact resistance and high reliability.

Means to solve the problem

The method for manufacturing a semiconductor device pertaining to the present invention involves a step in which a base layer provided with a lower aluminum wiring layer is prepared, a step in which an interlayer insulating film having contact holes at prescribed positions is formed on the aforementioned base layer, a step in which dry etching cleaning is applied to the aforementioned lower aluminum wiring layer exposed via the aforementioned contact holes using a mixed gas comprising a rare gas and a hydrogen gas, and a step in which an upper wiring layer is formed on the aforementioned interlayer insulating film while achieving electrical connection with the aforementioned lower aluminum wiring layer via the aforementioned contact holes.

Function

In the present invention, because the step in which dry etching cleaning is applied to the lower aluminum wiring layer exposed via the contact holes using a mixed gas comprising a rare gas and a hydrogen gas is provided, the degenerated layer formed on the surface of the lower aluminum wiring layer is removed by means not only of a physical method but also of a chemical method.

Application example

Figure 1 is a cross section of a semiconductor device created using an application example of the method for manufacturing a semiconductor device pertaining to the present invention.

Next, the method for manufacturing a semiconductor device shown in Figure 1 will be described. First interlayer insulating film 2, lower aluminum wiring layer 3, and second interlayer insulating film 4 with via-holes are formed on silicon substrate 1 using the same conventional method. At this time, degenerated layer 6 is formed on lower aluminum wiring layer 3 exposed by the via-hole parts, like in the past.

Next, when dry etching cleaning is applied to lower aluminum wiring layer 3 exposed by the via-hole parts using a mixed gas comprising an argon gas as a rare gas and a hydrogen gas, sputtering etching (physical method) with the plasma of the argon gas is realized, like in the past, and HF and water are created as the fluorine and the oxygen contained in the hydrogen gas and degenerated layer 6 react with each other (chemical method). Boiling point of HF is 19.5°C, and the boiling point of hydrogen is 100°C. Because the semiconductor manufacturing process is usually carried out under a temperature higher than said temperatures, the HF and water are removed as vapors. Thus, even when the particles of degenerated layer 6 removed during the sputtering etching adhere again, like in the past, they are removed completely by the chemical method.

Next, upper aluminum wiring layer 5 is formed on second interlayer insulating layer 4 while achieving electrical connection with lower aluminum wiring layer 3 through the via-holes using the same conventional method. At this time, because degenerated layer 6 that used to be present on the surface of lower aluminum wiring layer 3 at the via-holes is already removed completely, the contact resistance between lower aluminum wiring layer 3 and upper aluminum wiring layer 5 is not as high as in the past, so that the reliabilities of the electromigration tolerance and the stress migration tolerance do not deteriorate, either.

Furthermore, although a case in which the lower and the upper wiring layers are of aluminum wiring was shown in the aforementioned application example, the upper layer wiring does not have to be of aluminum wiring. Moreover, the rare gas is not limited to argon gas.

Effect of the invention

As described above, because the step in which dry etching cleaning is applied to the lower aluminum wiring layer exposed via the contact holes using the mixed gas comprising the rare gas and the hydrogen gas is provided, the degenerated layer formed on the surface of the lower aluminum wiring layer is removed by means not only of the physical method but also of the chemical method. As a result, the present invention offers an effect that the contact resistance between the upper aluminum wiring layer and the lower aluminum wiring layer is reduced, and the reliabilities of the electromigration tolerance and the stress migration tolerance at the via-holes are improved.

Brief description of the figures

Figure 1 is a diagram for explaining the application example of the method for manufacturing a semiconductor device pertaining to the present invention, and Figure 2 is a diagram for explaining the conventional method for manufacturing semiconductor devices.

In the figures, 3 indicates the lower aluminum wiring layer, 4 indicates the second interlayer insulating film, and 5 indicates the upper aluminum wiring layer.

Furthermore, in the figures, the same symbols indicate the same parts or equivalents.

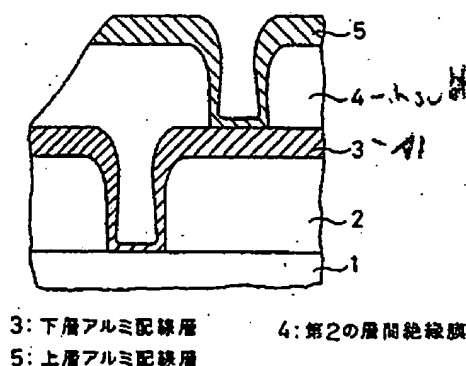


Figure 1

- Key: 3 Lower aluminum wiring layer
 4 Second interlayer insulating film
 5 Upper aluminum wiring layer

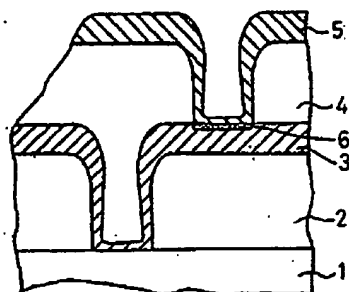


Figure 2



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APPLICANTS

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GIRISH A. DIXIT, PLANO, TX;

** CONTINUING DATA *****

** FOREIGN APPLICATIONS *****

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** 03/18/1998

Foreign Priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no	STATE OR COUNTRY TX	SHEETS DRAWING 3	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 3
35 USC 119 (a-d) conditions met <input type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after Allowance				
Verified and Acknowledged	Examiner's Signature	Initials		

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23494

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TITLE

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